

# Monolithic Electronics for Multi-channel Detectors

Paul O'Connor, Brookhaven National Laboratory

Workshop on position-sensitive Neutron Detectors, June 28 – 30,  
2001

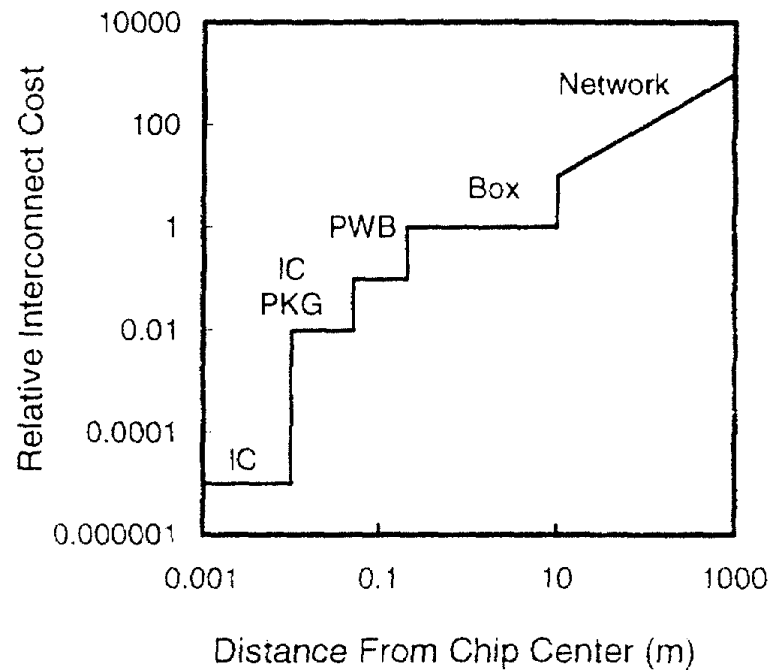
# Outline

- Monolithic circuits for scientific research
- Technology selection and access
- Preamplifier and shaping amplifier design
- Impact of scaling
- BNL preamp/shaper examples
- Sampling systems
- Peak detection and derandomization
- Summary and future directions

# Monolithic Front Ends

- Can be efficiently mass-produced with excellent economy of scale:
  - E.g., maskset + 10 wafers ~ \$100K, 500 chips/wafer
  - Additional wafer ~ \$5K
  - Incremental cost ~ \$10/chip
  - Chip may have 16 – 128 channels
- Can be located close to dense detector electrode arrays
  - pixels, micropattern & segmented cathode designs
- Can combine functions on single chip, replacing PCB/hybrid/cable connections with lower cost on-chip connection
- Can reduce power\*

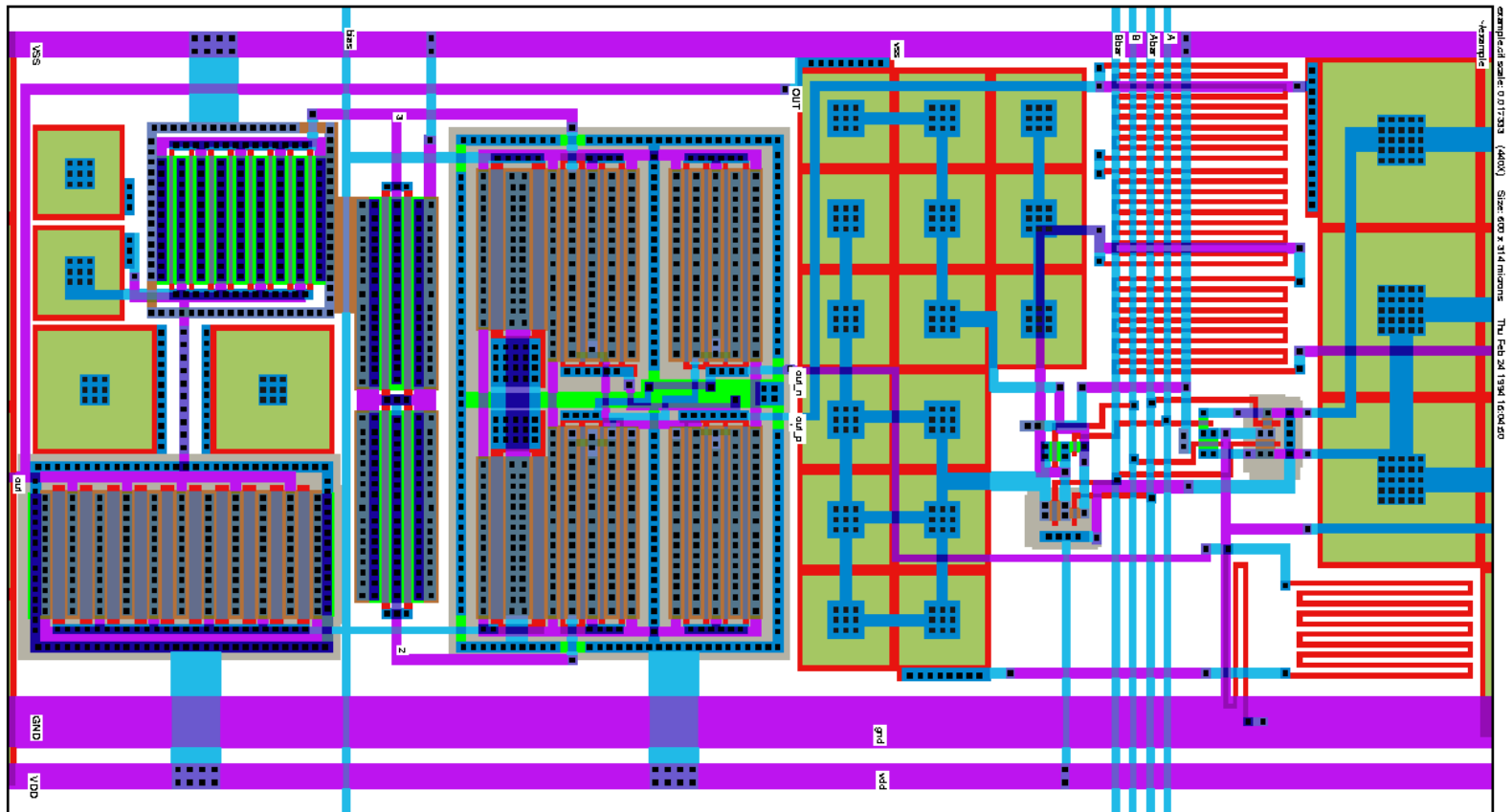
# Cost of Interconnect



# Custom Monolithics – technology options

- **Bipolar**
  - Workhorse of “old” analog
  - Available from a handful of vendors
  - Speed/power advantage over CMOS (diminishing)
  - Low integration density
- **Standard CMOS**
  - Suitable for most analog designs
  - Best for combining analog and digital
  - Highest integration density
  - Widely available
  - Short life cycle (3 years/generation)
- **BiCMOS**
  - Complex process, viability uncertain
- **Silicon on insulator (SOI)**
  - Modest speed advantage for digital
  - Drawbacks for analog
- **SiGe**
  - Complexity equivalent to BiCMOS
  - Extremely fast bipolar device plus submicron CMOS
  - Availability increasing
- **GaAs**
  - Unsuitable for wideband analog

# Analog CMOS layout



# Access to Monolithic Processes

## **Multiproject (shared wafer) foundry runs**

*In the U.S.*

MOSIS service [www.mosis.org](http://www.mosis.org)

*Europe*

Europractice [www.imec.be/europractice](http://www.imec.be/europractice)

## **Design tools**

*Public domain*

MAGIC

[bach.ece.jhu.edu/~tim/programs/magic/magic7.html](http://bach.ece.jhu.edu/~tim/programs/magic/magic7.html)

[vlsi.cornell.edu/magic](http://vlsi.cornell.edu/magic)

*Commercial*

Cadence [www.cadence.com](http://www.cadence.com)

Mentor [www.mentor.com](http://www.mentor.com)

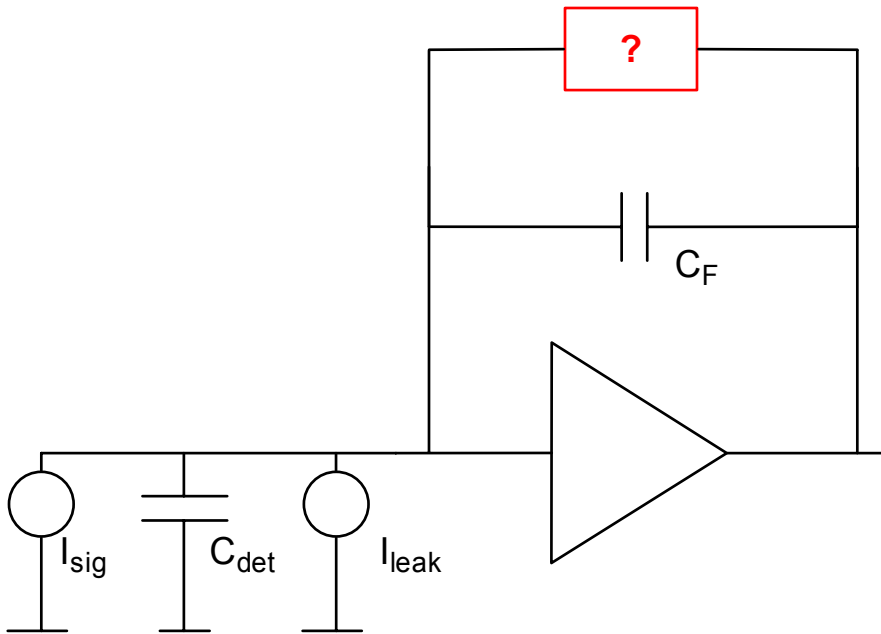
Tanner [www.tanner.com](http://www.tanner.com)

# Preamplifier Design: Front Transistor Optimization

- For MOSFETs, the input device must be properly dimensioned to match  $C_{\text{det}}$ :
  - 1/f noise minimized for  $C_{\text{gs}} = C_{\text{det}}$
  - Series thermal noise minimized for  $C_{\text{gs}} < C_{\text{det}}$ , exact value depends on  $C_{\text{det}}/I_{\text{d}}$
- For Bipolar transistors, must choose the collector current
  - Depends on  $C_{\text{det}}/t_{\text{m}}$
- MOS will have superior noise when
  - $t_{\text{m}}/\tau_{\text{el}} > \beta_{\text{BJT}}$
  - $kT/K_{\text{F}} > \beta_{\text{BJT}}$
- Bipolar favored for short shaping, low power.

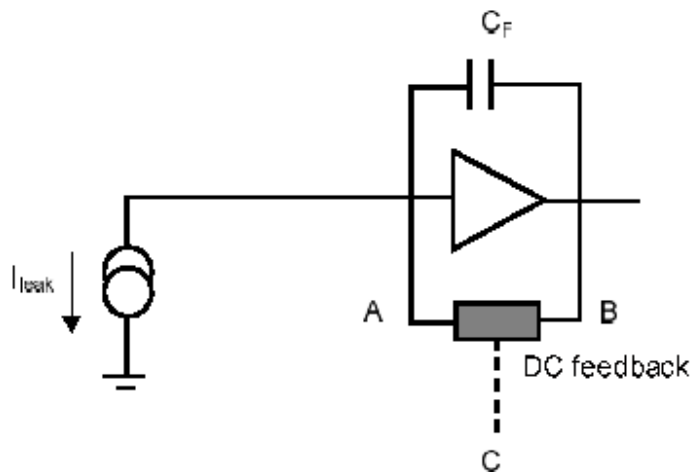


# Preamp Reset – Requirements



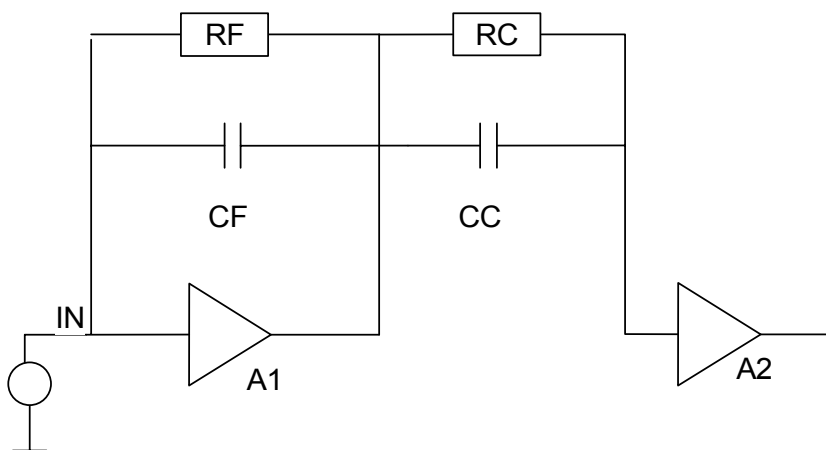
- all charge preamplifiers need DC feedback element to discharge  $C_F$
- usually, a resistor in the  $M\Omega - G\Omega$  range is used
- monolithic processes don't have high value resistors
- we need a circuit that behaves like a high resistor and is also
  - insensitive to process, temperature, and supply variation
  - low capacitance
  - lowest possible noise
  - linear

# Preamp Reset – Configurations



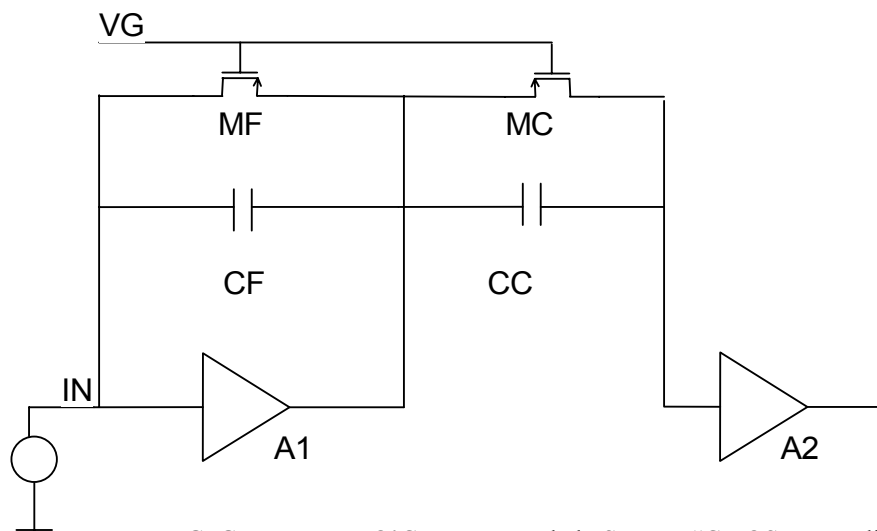
Feedback type	Circuit	$R_{eff} (I_{leak} = 0)$	Advantages/ Disadvantages
Physical resistor	A  B	$R$	+ simple - hard to make large R - parasitic C - doesn't adjust to $I_{leak}$
MOS switch	A  B C(pulse)	$\frac{1}{C_F \cdot f_{reset}}$	+ simple - dead time - switch noise
Triode MOS	A  B C Bias	$\frac{1}{\beta \cdot (V_{gs} - V_T)}$	+ compact + adjusts to $I_{leak}$ - nonlinear
Feedback $g_m$	A  B $g_m$ C (Vref)	$\frac{1}{g_m}$	+ adjusts to $I_{leak}$ - complex - excess noise - nonlinear
Attenuating current mirror	A  B $A_i \ll 1$	$\frac{R}{A_i}$	+ aux. output for PZC - doesn't adjust to $I_{leak}$

# Nonlinear Pole-zero Compensation



- Classical

- $RF \cdot CF = RC \cdot CC$
- Zero created by RC, CC cancels pole formed by RF, CF



- IC Version

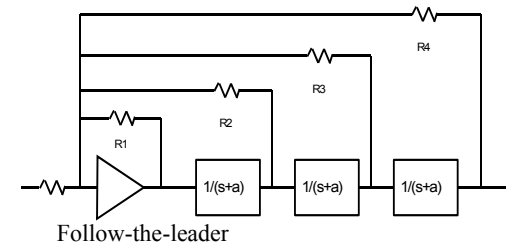
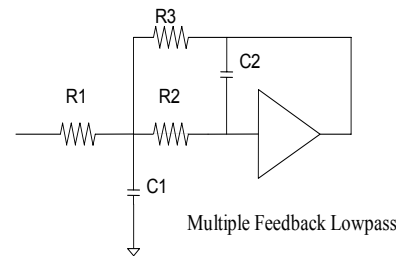
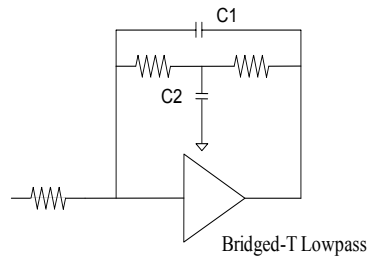
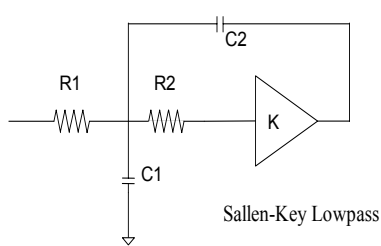
- $CC = N \cdot CF$
- $(W/L)_{MC} = N \cdot (W/L)_{MF}$
- Zero created by MC, CC cancels pole formed by MF, CF
- Rely on good matching characteristics of CMOS FETs and capacitors

G. Gramegna, P. O'Connor, P. Rehak, S. Hart, "CMOS preamplifier for low-capacitance detectors", NIM-A 390, May 1997, 241 – 250.

# Pulse Shaping with Monolithic Circuits

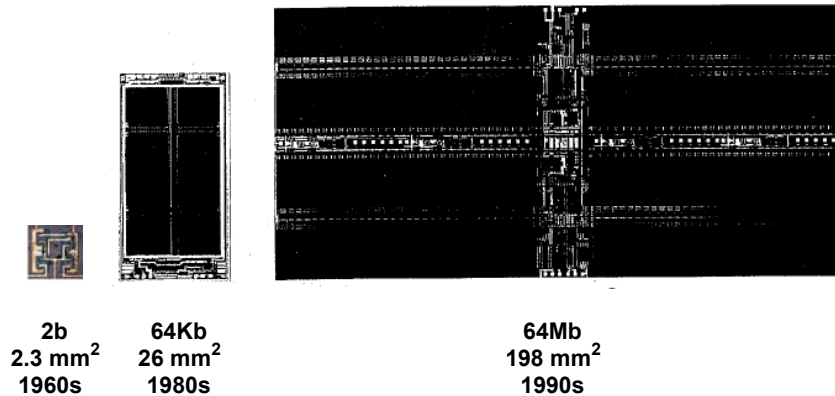
- Passive components in monolithic technology are non-ideal:
  - Tolerance typically  $\pm 20\%$  from lot to lot.
  - Values restricted to  $C < 50 \text{ pF}$ ,  $R < 100\text{K}$ .
  - Difficulty in setting accurate filter time constants
- Low supply voltage in submicron CMOS (1.8 – 3.3V)
  - Restricts dynamic range
- Feedback circuits give the most stable and precise shaping
  - But require more power than other approaches

## Filter topologies



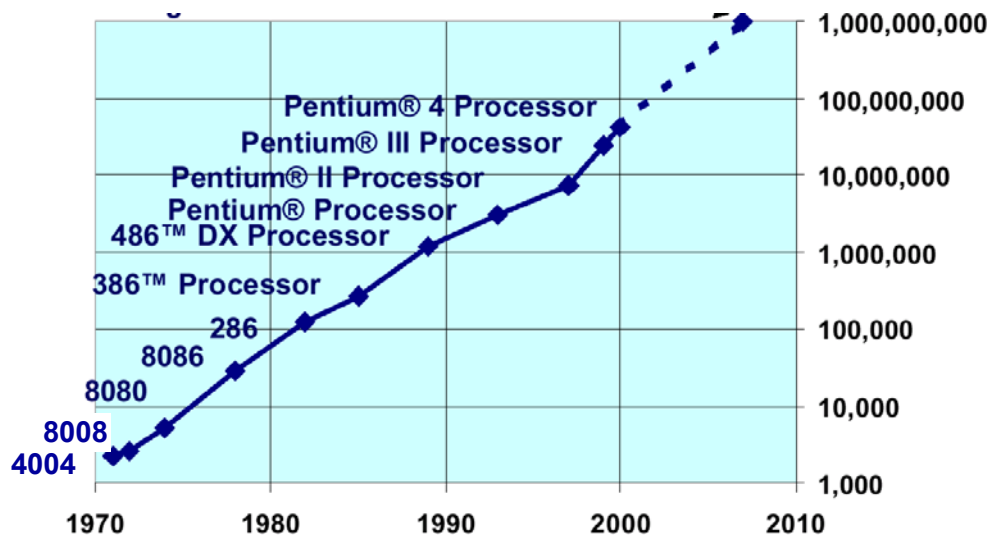
# CMOS Scaling

## DRAM



- Driven by digital VLSI circuit needs
- Goals: in each generation
  - 2X increase in density
  - 1.5X increase in speed
  - Control short channel effects
  - Maintain reliability level of  $< 1$  failure in  $10^7$  chip-hours

## Intel microprocessor

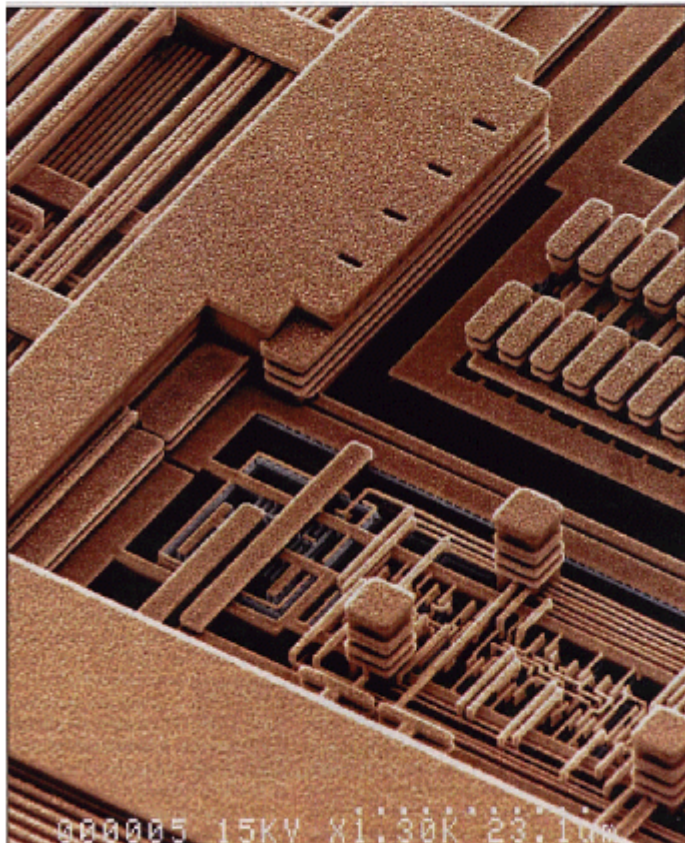


# CMOS Technology Roadmap

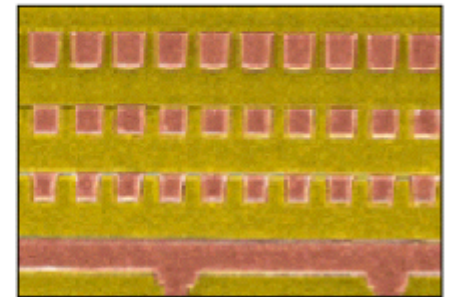
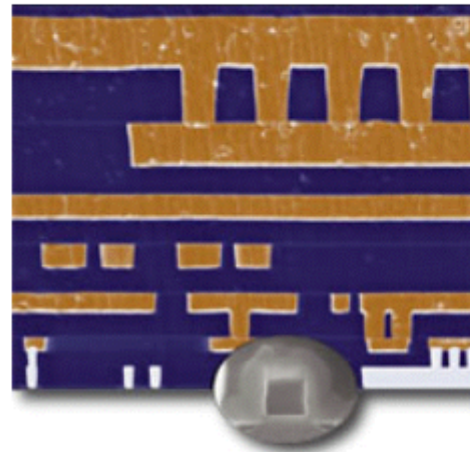
Year	85	88	91	94	97	00	02	04	07	10	13
Min. feature size [ $\mu\text{m}$ ]	2	1.5	1.0	0.7	0.5	0.35	0.25	0.18	0.13	0.10	0.07
Gate oxide [nm]	44	33	22	16	11	7.7	5.5	4.0	2.9	2.2	1.6
Power supply [V]	5	5	5	5	5/3.3	3.3	2.5	1.8	1.2	1	.7
Threshold voltage [V]	1.0	0.9	0.8	0.7	0.6	0.5	0.45	0.4	0.3	0.3	0.3



## IBM Cu-11 Process (Blue Logic)



[1] IBM Corp.'s new CMOS 7S process for manufacturing ICs uses copper for its six levels of interconnections, and has effective transistor channel-lengths of only 0.12  $\mu\text{m}$ . It is the first commercial fabrication process to use copper wires [see "The Damascus connection," p. 25].



Section showing Cu-11 copper and low-k dielectric process.

- $L_{\text{eff}} = 0.08 \mu\text{m}$ ,  $L_{\text{drawn}} = 0.11 \mu\text{m}$
- Up to 40 million wireable gates
- Trench capacitor embedded DRAM with up to 16 Mb per macro
- Dense high-performance, compact SRAMs
- Power supply: 1.2 V with 1.5 V opt on
- I/O power supply: 3.3 V (dual oxide option)/2.5 V (dual oxide option)/1.8 V/1.5 V
- Power dissipation of 0.009  $\mu\text{W}/\text{MHz}/\text{gate}$
- Gate delays of 27 picoseconds (2-input NAND gate)
- Seven levels of copper for global routing
- Low-k dielectric for high performance and reduced power and noise
- HyperBGA (flip chip): 2577 total leads

# CMOS scaling and charge amplifier performance

- Fundamental noise mechanisms
  - so far, no dramatic changes with scaling
- Noise
  - slight improvement with scaling
  - higher device  $f_T$  reduces series thermal noise
- Weak- and moderate inversion operation more common
  - need different matching to detector capacitance.
- Reduced supply voltage
  - difficult to get high dynamic range
- Many difficulties with “end of the roadmap” devices



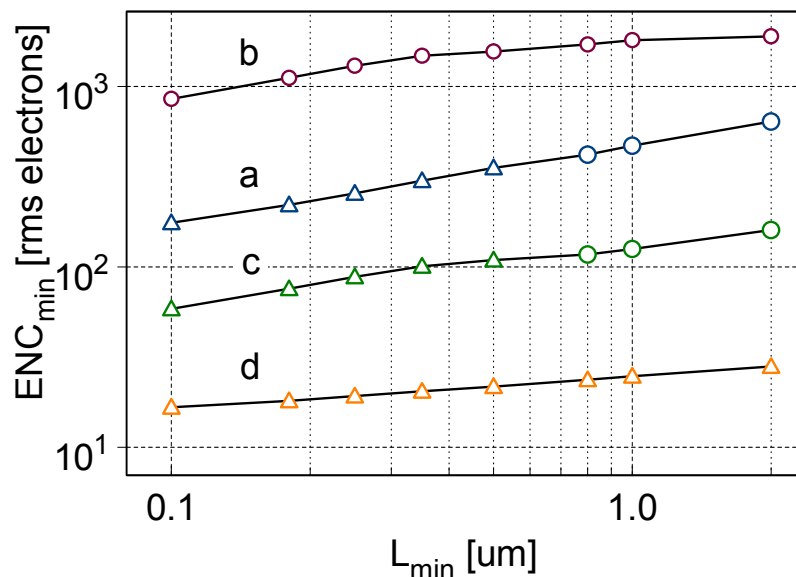
# Impact of technology scaling on charge amplifier performance

4 detector scenarios for scaling study

System	$C_{det}$	$t_{re}$	P	$I_{leak}$	Detector	Typical Application
a	30	75	10	.001	Wire Chamber	Tracking, Imaging
b	15	25	0.2	10	Si Strip	Tracking
c	0.3	25	0.02	1	Si Pixel	Tracking
d	3	2500 – 500*	10	0.01	Semiconductor	Spectroscopy
UNITS	pF	ns	mW	nA	-	-

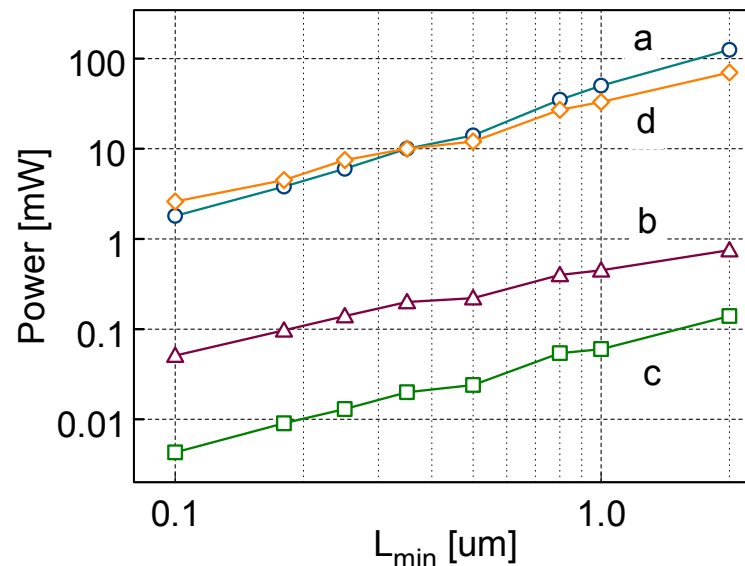
Noise vs. scaling

(power held constant)



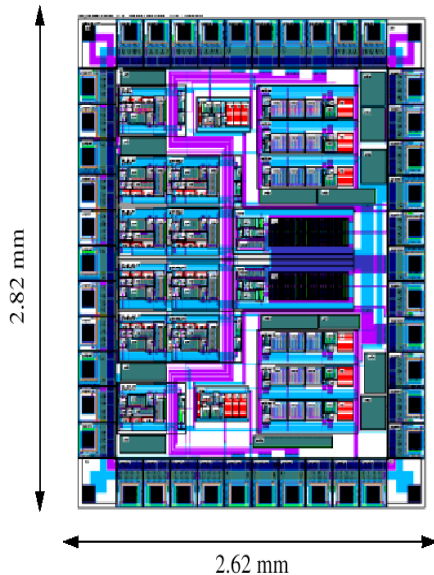
Power vs. scaling

(noise held constant)

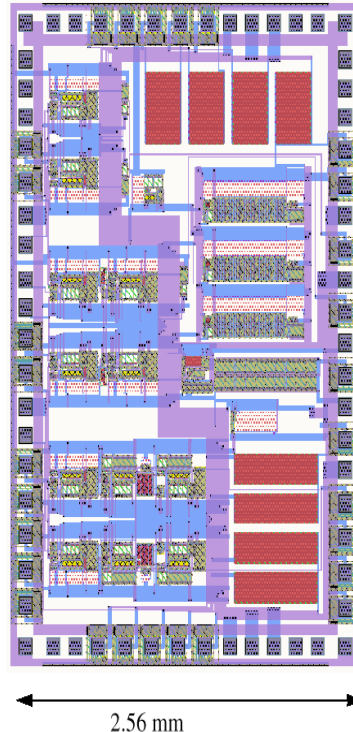


# Drift Detector Preamplifier

HP 1.2um version



AMS 1.2um version

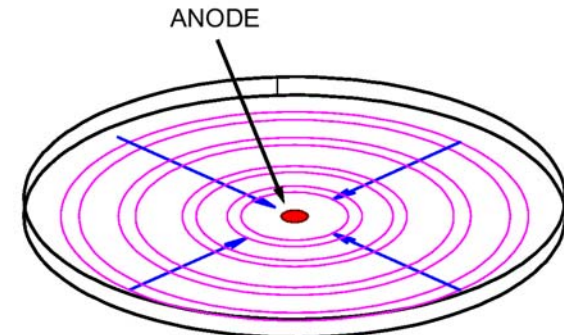


Requirements for 100 eV resolution with a 0.2 pF detector at 1 - 5  $\mu$ s shaping time:

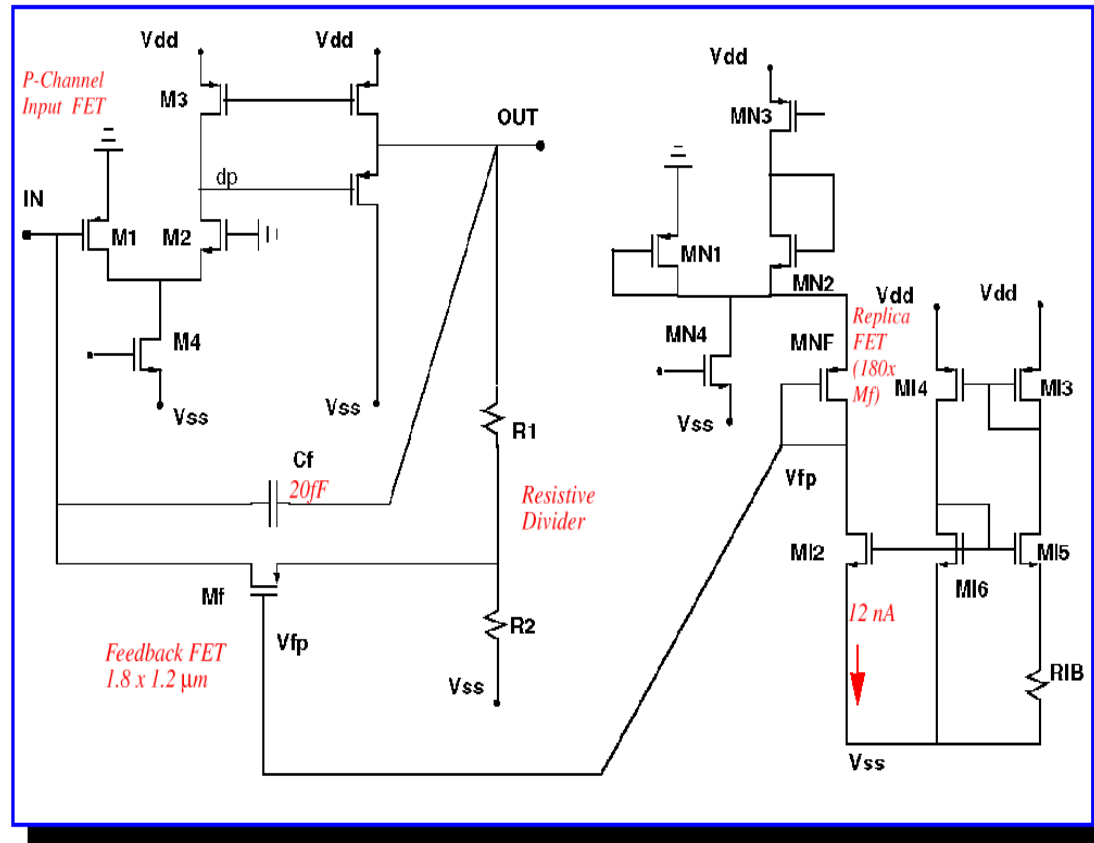
- $I_{leak} < 10$  pA
- $R_F > 3$  G $\Omega$
- $g_m > 0.4$  mS
- $K_F < 1.8 \times 10^{-25}$  J

- Used with ultra-low capacitance silicon drift detector,  $C_{det} < 0.3$  pF
- Preamp only, used with external shaper
- Purpose: explore lowest noise possible with CMOS
- Reset system: MOS transistor with special bias circuit to achieve stable,  $> 100$  G $\Omega$  equivalent resistance

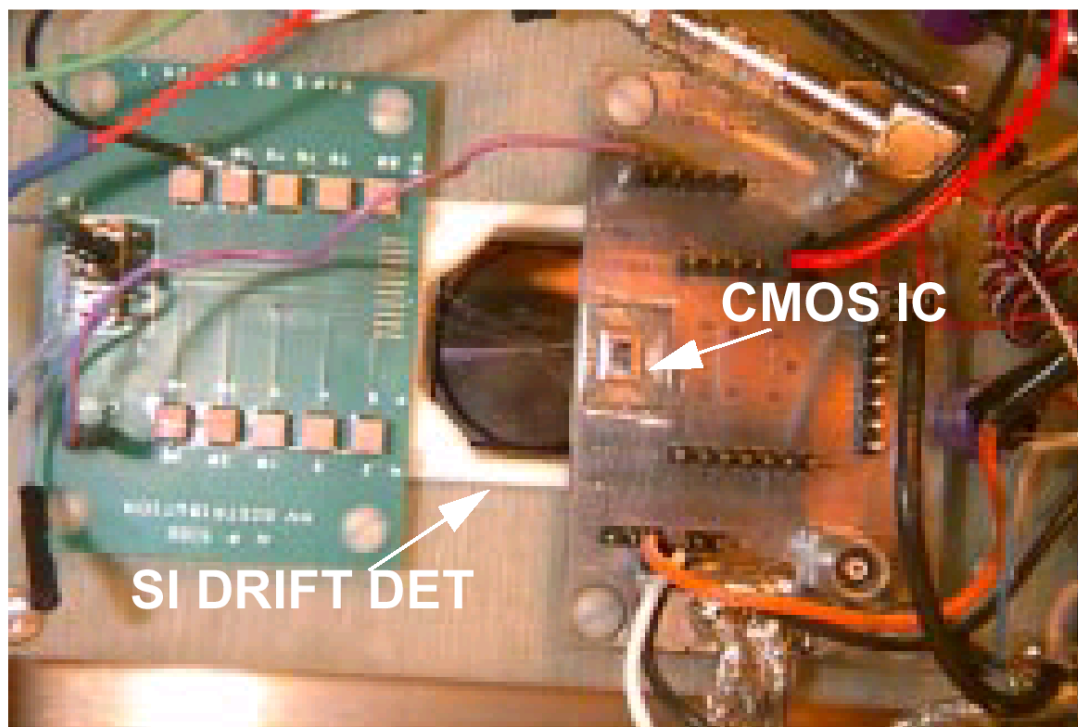
Detector



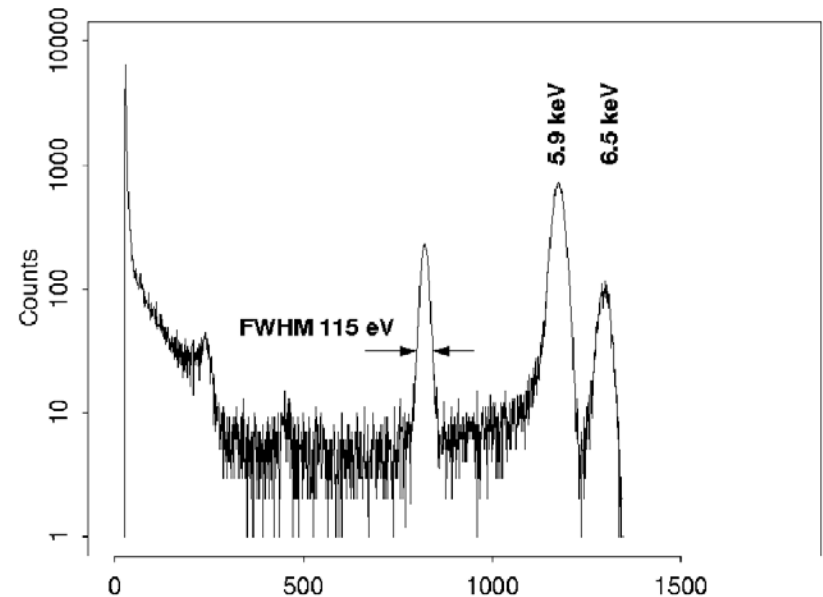
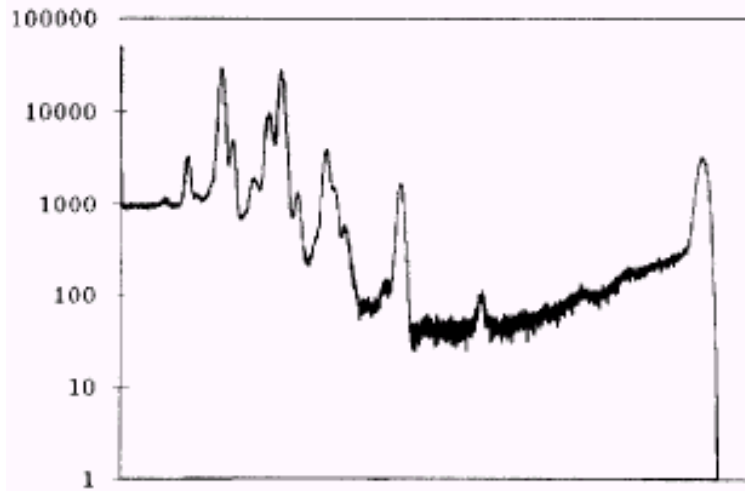
# Drift detector preamplifier – simplified schematic



# Drift Detector & CMOS Preamplifier



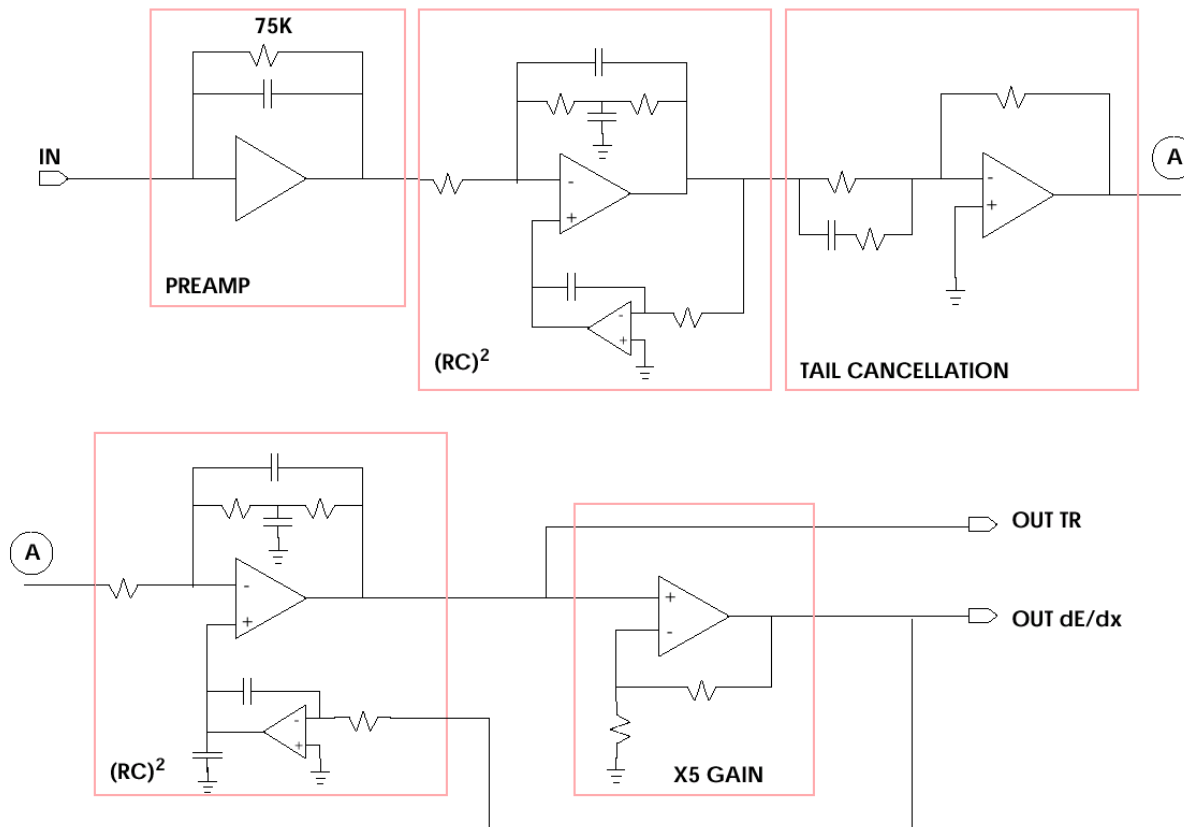
# Drift detector preamplifier – results



- Spectra of  $^{241}\text{Am}$  and  $^{55}\text{Fe}$  taken with 5mm  $\Phi$  Si drift detector and CMOS X-ray preamplifier. Detector and circuit cooled to  $-75^\circ\text{C}$ .
- External 2.4  $\mu\text{s}$  shaping.
- ENC = 13  $e^-$  rms.
- Noise without detector: 9  $e^-$

# Time Expansion Chamber & Transition Radiation Detector

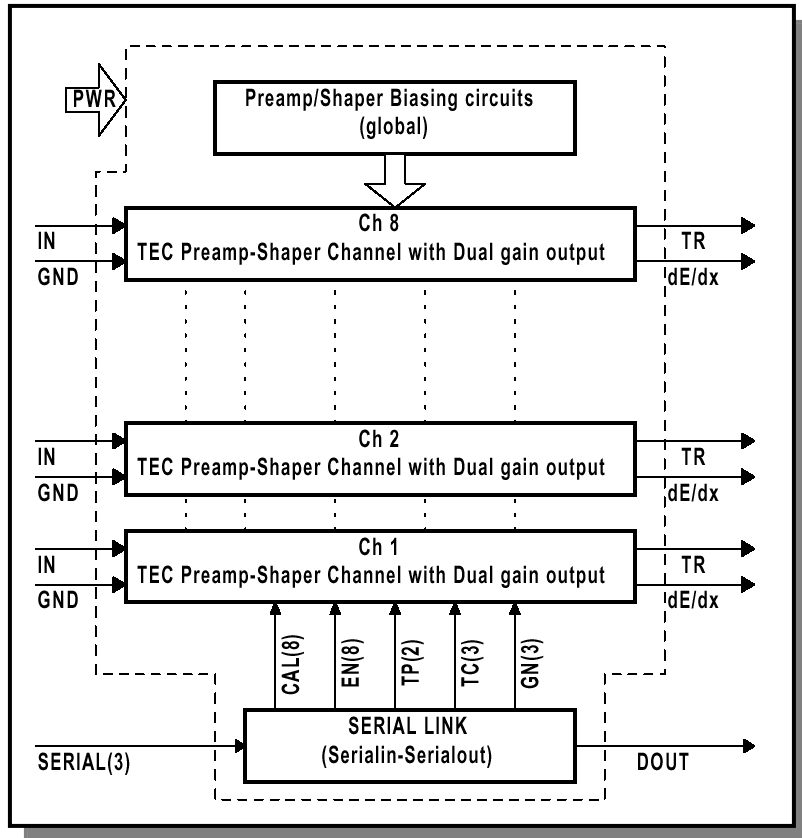
## Preamp/Shaper



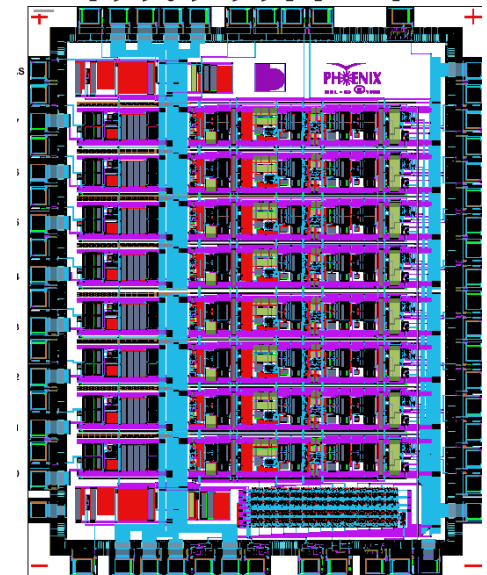
- 1m MWPC with 20 pF  $C_{DET}$
- Fast (70 ns) shaping for charged particle tracking
- Dual gain outputs for measurement of dE/dx and Transition Radiation

# TEC-TRD Preamp/Shaper

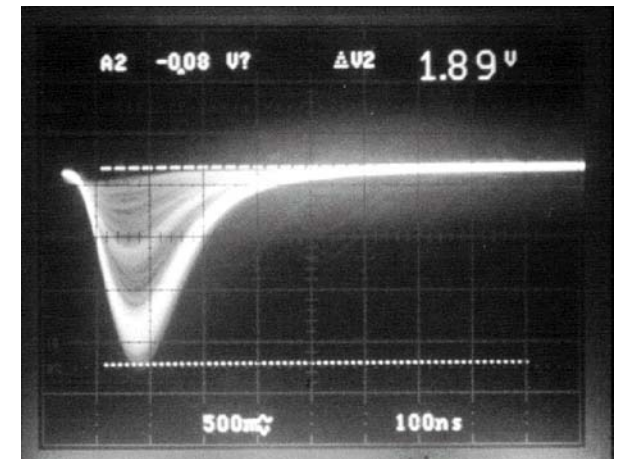
## Block Diagram



## Die Layout



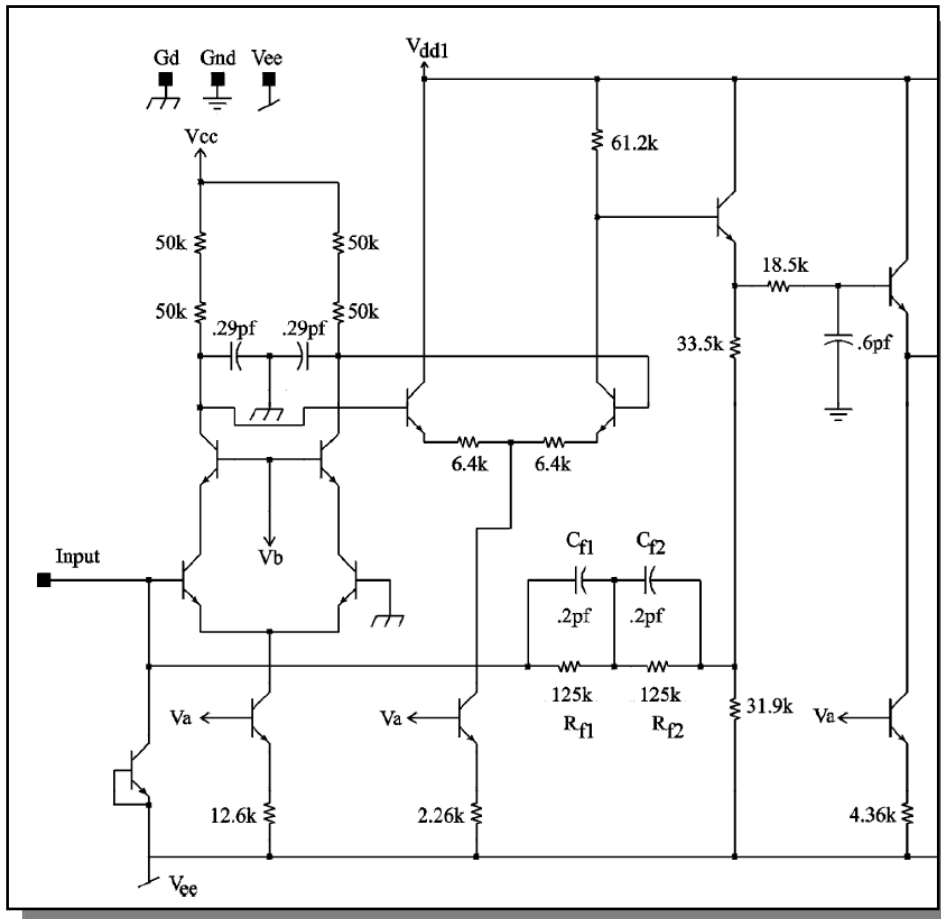
## X-ray Response



A. Kandasamy, E. O'Brien, P. O'Connor, W. VonAchen, "A monolithic preamplifier-shaper for measurement of energy loss and transition radiation" IEEE Trans. Nucl. Sci. 46(3), June 1999, 150-155

# Silicon Vertex Tracker

## Preamplifier/Shaper

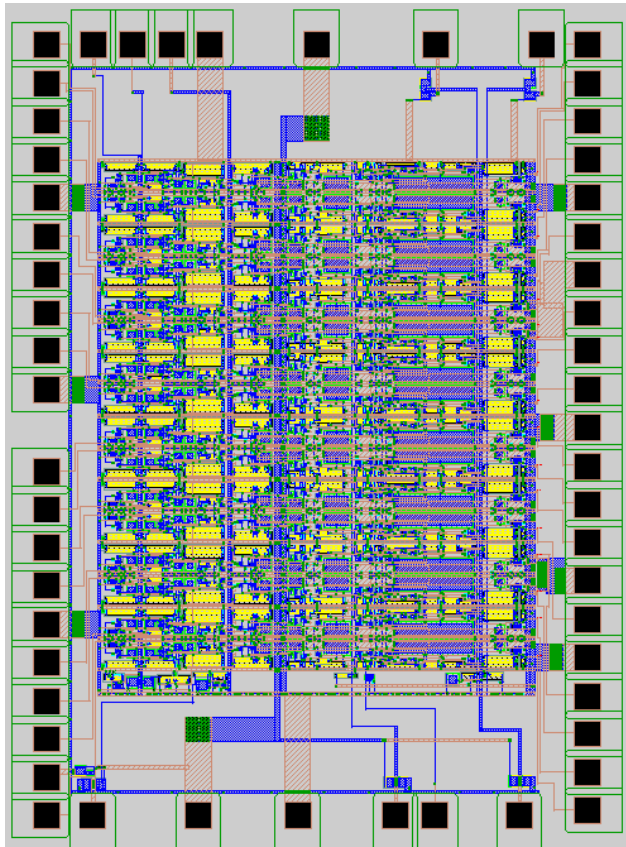


- Direct connection to low-capacitance (3 pF) silicon drift detector
- Fast shaping (50 ns) for tracking
- Low power requirement (< 5 mW/chan.)
- Silicon bipolar technology

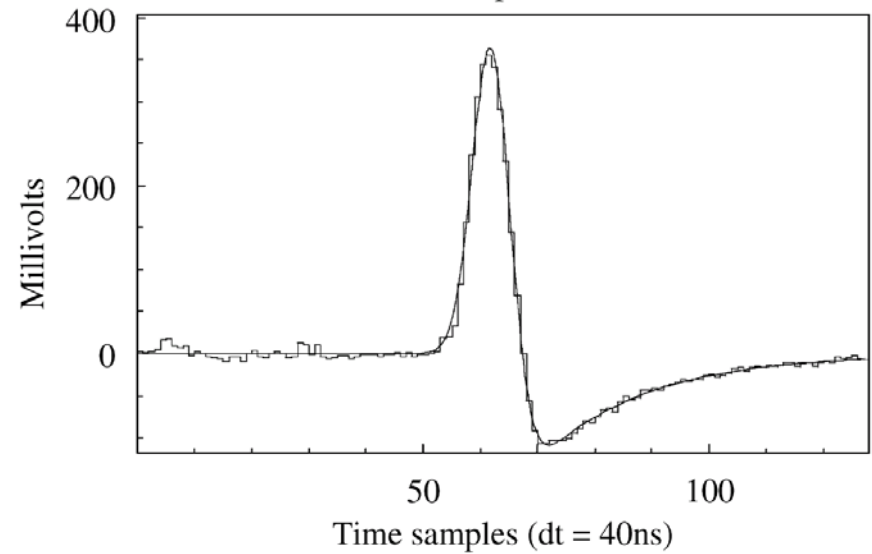


# SVT Preamp/Shaper

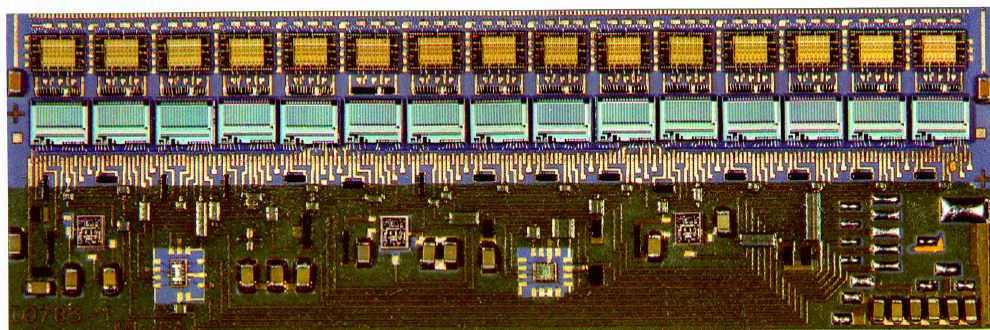
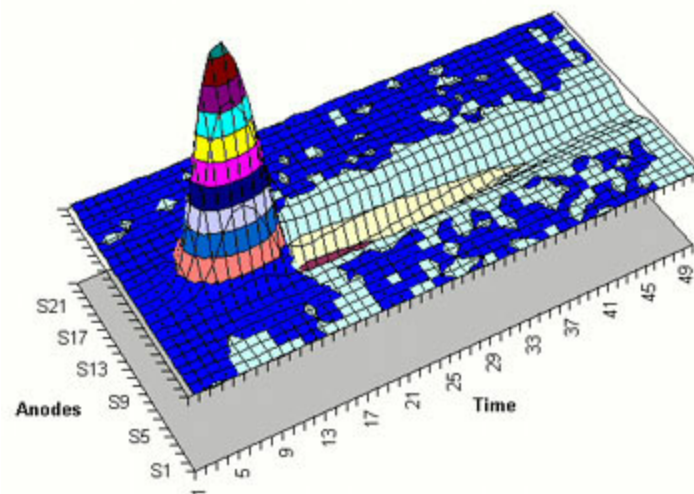
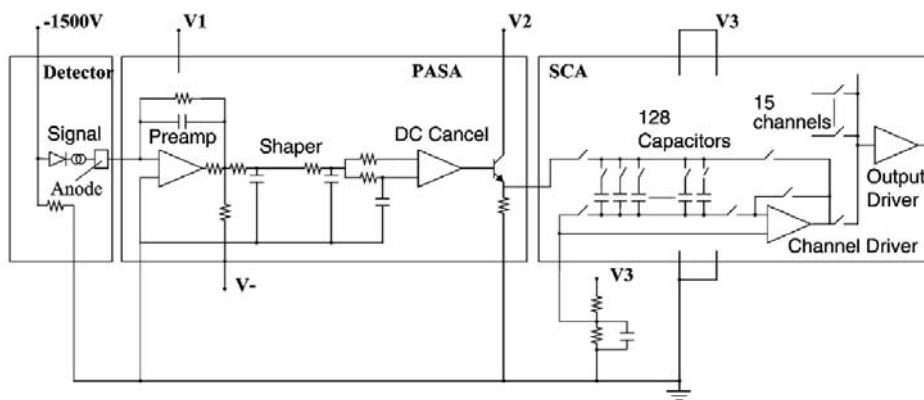
Die Layout



Output Waveform



# SVT 240-channel Multi-Chip Module



D. Lynn et al., "A 240 channel thick film multi-chip module for readout of silicon drift detectors", NIM A439 (2000), 418 - 426

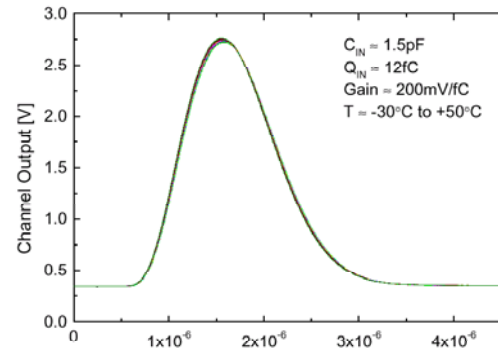
# BNL Preamp/Shaper ICs, 1995 - 2001

PROJECT	Hi-res. Spectroscopy	RHIC - PHENIX	RHIC - STAR	LHC - ATLAS	Industry Partnership	NSLS - HIRAX	Units
DETECTOR	Si drift	Time Expansion Chamber	Silicon Vertex Tracker	Cathode Strip Chamber	CdZnTe gamma ray detector	Si Pixel	
Function	Preamp	Preamp/Shaper	Preamp/Shaper	Preamp/Shaper	Preamp/Shaper	Preamp/Shaper/ Counter	
C <sub>DET</sub>	0.3	30	3	50	3	1.5	pF
Peaking Time	2400	70	50	70	600:1200:2000:4 000	500:1000:2000:4 000	ns
Gain	10	2.4:12 - 10/25	40:70:90	4	30:50:100:200	750:1500	mV/fC
Power	10	30	3.8	33	18	7	mW/channel
ENC	10	1250	400	2000	100	24	rms electrons
Dynamic Range	1250	4600	700	1900	5600		
Technology	CMOS 1.2 um	CMOS 1.2 um	Bipolar 4 GHz	CMOS 0.5 um	CMOS 0.5 um	CMOS 0.35 um	
Input Transistor	PMOS 150/1.2 um	NMOS 4200/1.2 um	NPN 10 uA	NMOS 5000/0.6 um	NMOS 200/0.6 um	PMOS 400/0.4 um	
Reset Scheme	Compensated PMOS, > 1G $\Omega$	Polysilicon, 75 k $\Omega$	Nwell, 250 k $\Omega$	Compensated NMOS, 30 M $\Omega$	Compensated PMOS	Compensated NMOS	
No. Channels	6	8	16	24	16	32	
Die Size	7.3	15	8	20	19	16	mm <sup>2</sup>

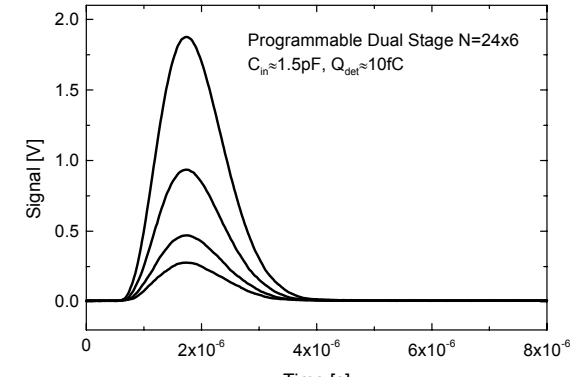
# Practical amplifier considerations

- Preamplifier reset
- High order filters
- Programmable pulse parameters
- Circuit robustness:
  - Self-biasing
  - Low-swing, differential I/O
  - Circuits tolerant to variations in
    - Temperature
    - Process
    - Power supply
    - DC leakage current
    - Loading

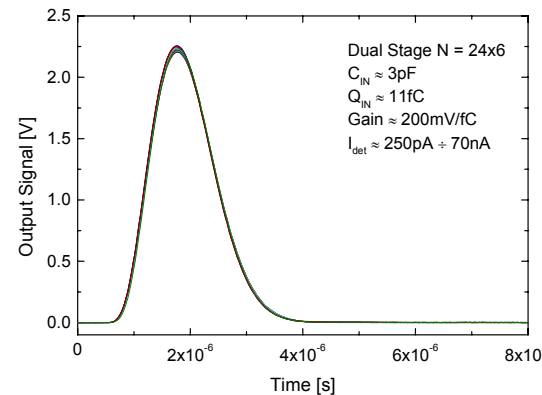
Pulse vs. Temperature



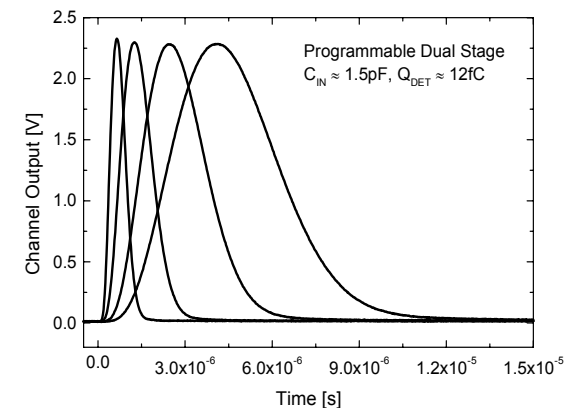
Gain variation



Pulse vs.  $I_{leak}$

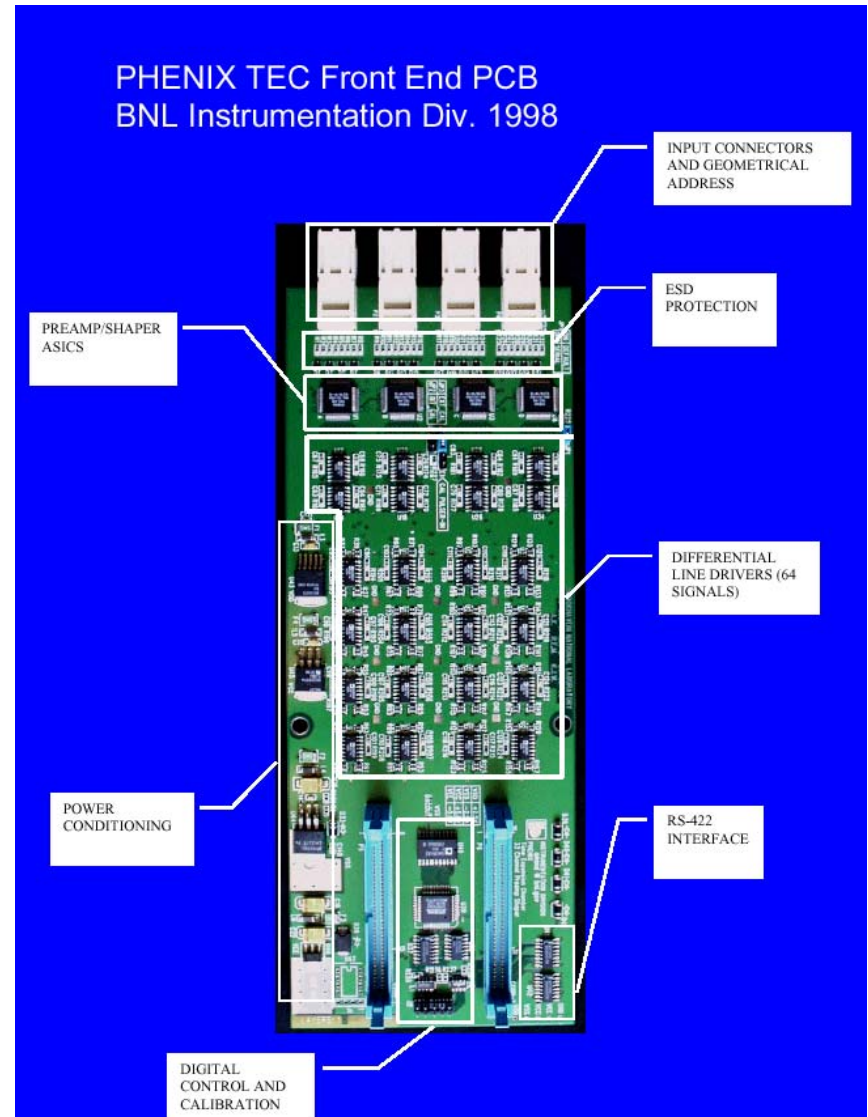
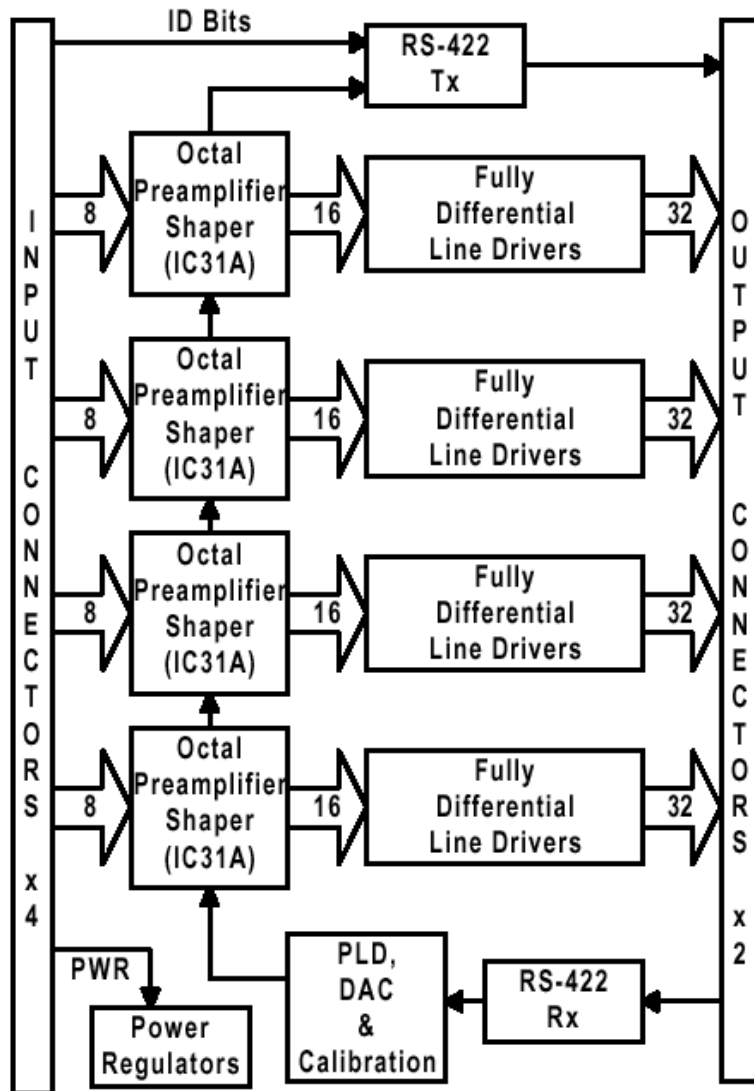


Peaking time variation



	$I_{leak}$	Supply	Temperature	Rate (to 5/tp)	Cin	Zload
Gain	$< 0.1\%/nA$	$< 0.001\%/V$	$-0.04\%/^\circ\text{C}$	$< 0.1\%$	$< 0.1\%/pF$	No slew-rate limit
Baseline	$< 0.3\text{mV}/nA$	$< 30 \mu\text{V}/V$	$75 \mu\text{V}/^\circ\text{C}$	$< 8 \text{mV}$	-	$Z_{out} \sim 150 \Omega$

# TEC Front-End Card

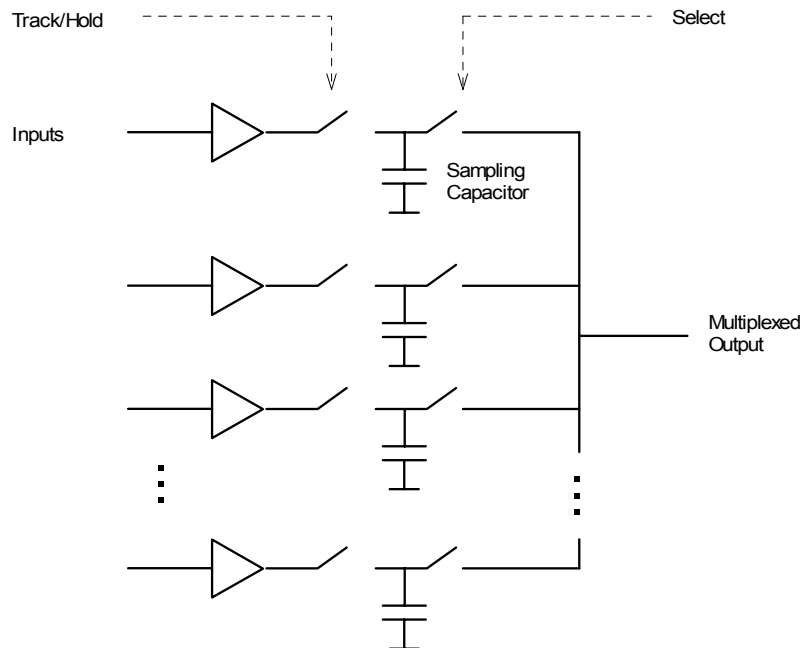


# What goes between the preamp/shaper and the ADC?

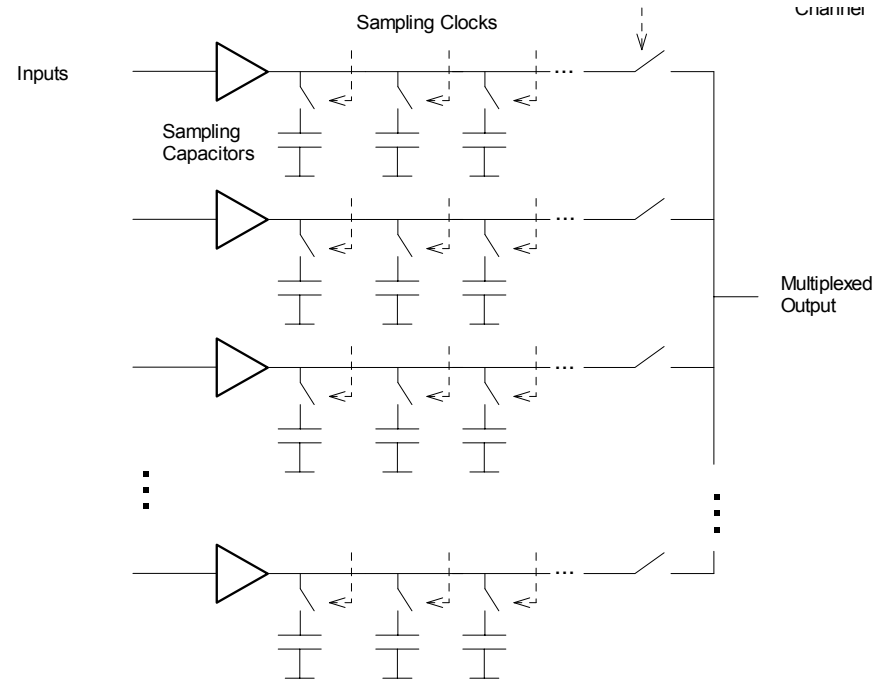
- Experimental needs differ
  - number of channels
  - occupancy
  - rate
  - trigger
- Usually, its too expensive to put an ADC per channel
- Anyway the ADC would usually not be doing anything useful
  - Occupancy < 100%, so no events most of the time in most channels
- What is the most efficient way to use the ADC(s)?

# Analog Sampling and Multiplexing

Track-and-hold  
(triggered systems)



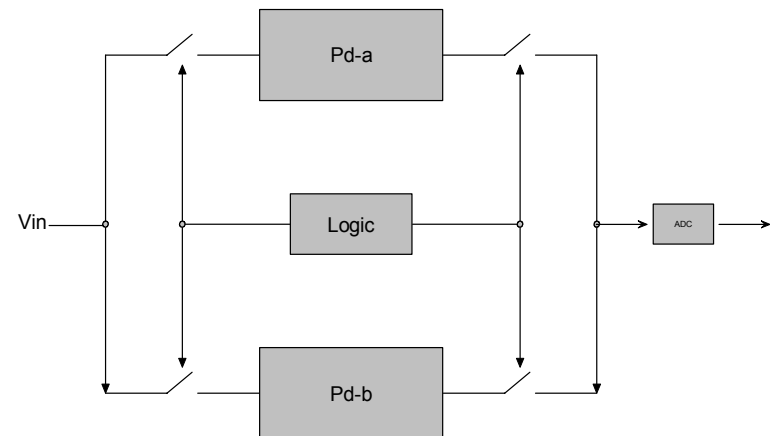
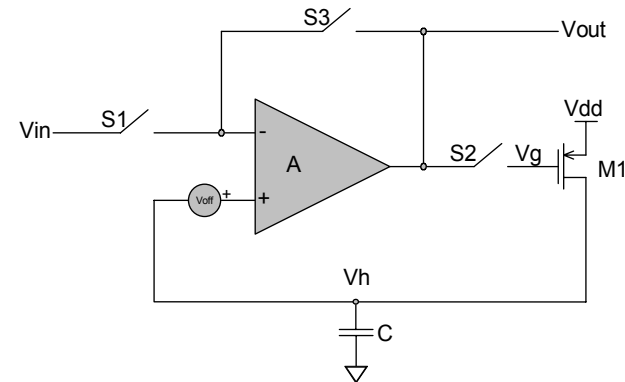
Analog memory  
(non-triggered)





# New Peak Detector and Derandomizer

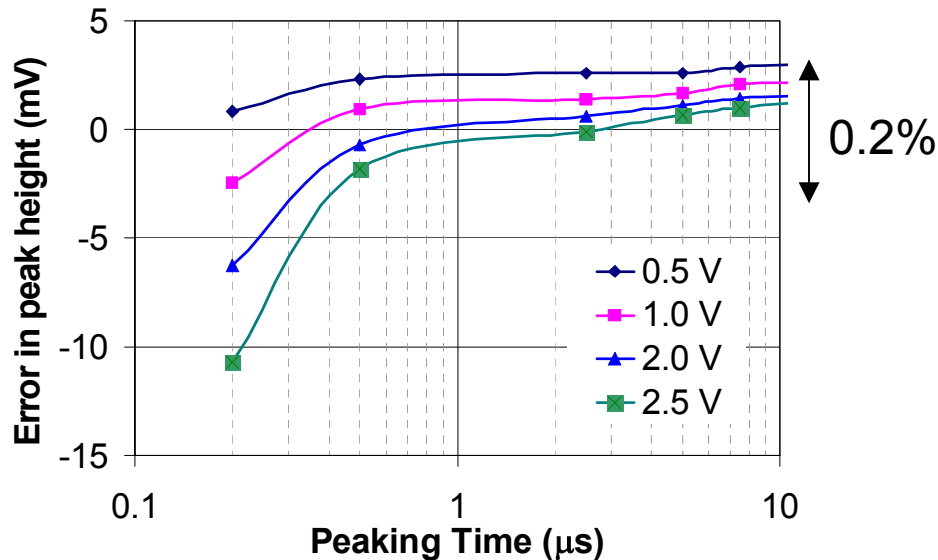
- Self-triggered
- Self-sparsifying
- New 2-phase configuration allows rail-to-rail operation, eliminates offsets
  - absolute accuracy  $\sim 0.2\%$
  - to within 300 mV of rails
- Two or more peak detectors in parallel can be used to derandomize events
  - If a second pulse arrives before the readout of the first pulse in Pd-a, it is detected and stored on Pd-b.



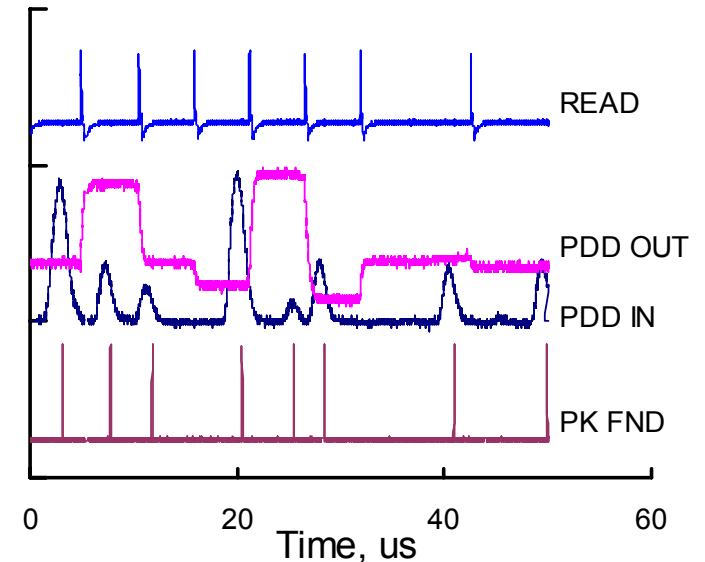


# First experimental results

Accuracy of single PD



PD/D response to random pulse train ( $^{241}\text{Am}$  on CZT)



G. DeGeronimo, P. O'Connor, A. Kandasamy, "Analog Peak Detect and Hold Circuits Part 2: The Two-Phase Offset-Free and Derandomizing Configurations", NIM-A submitted for publication

# Summary and Future Directions

- Today's monolithic technology can be used effectively for low-noise front ends.
- Technology scaling, by reducing the area and power per function, will allow increasingly sophisticated signal processing on a single die.
- Integrated sensors will be developed for some X-ray and charged-particle tracking applications.
- Interconnecting the front end to the detector and to the rest of the system will continue to pose challenges.